

# MF4SAM3

## MIFARE SAM AV3 secure access module

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Product short data sheet

COMPANY PUBLIC

## 1 General description

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The NXP MIFARE SAM AV3 secure hardware solution is the ideal add-on for reader devices offering additional security services. Supporting DES, TDEA, AES and RSA capabilities, it offers secure storage and secure communication in a variety of infrastructures.

Unlike other products in the field, MIFARE SAM AV3 has proven interoperability with all of NXP's broad card and RFID product portfolio, (MIFARE, NTAG DNA, ICODE DNA, UCODE DNA and SmartMX product families), making it the most versatile and secure SAM solution on the market today.

The MIFARE SAM AV3 is built on NXP's SmartMX2 P60 secure smart card controller with CC EAL6+ certification. Its software implementation is evaluated and composite certified by the MIFARE Security Evaluation Scheme. Similar to the hardware CC evaluation, the MIFARE Scheme also evaluates against high attack potential. Hence, systems using MIFARE SAM AV3 are reassured with the state-of-the-art security measures adopted by the industry.

### **Programmable Logic**

The MIFARE SAM AV3 is equipped with a new Programmable Logic functionality which allows customers to flexibly create their business logic on the SAM. This new functionality opens up many new possibilities with the creation of project-specific customization such as a new key diversification algorithm, a new secure messaging, or a new secure storage.

### **X-mode communication**

When used in combination with a reader IC supporting innovative "X" features, MIFARE SAM AV3 provides a significant boost in performance to the reader along with faster communication between reader and module. The "X" feature is a new way to use the SAM in a system, with SAM connected to the microcontroller and the reader IC simultaneously.

### **Secured communication**

The connection between the SAM and the reader is performed using security protocols based on either AES symmetric cryptography or PKI RSA asymmetric cryptography. The protocols comply with the state-of-art standards and thereby ensure data confidentiality and integrity.



## 2 Features and benefits

### 2.1 Cryptography

- Supports MIFARE Crypto1, DES, TDEA (112 and 168 bits), AES (128, 192 and 256 bits), RSA (up to 2048 bits) and ECC (up to 256 bits) cryptography
- Supported NXP's products:
  - MIFARE DESFire, MIFARE DESFire EV1, MIFARE DESFire EV2
  - MIFARE Plus, MIFARE Plus EV1
  - MIFARE Classic, MIFARE Classic EV1
  - MIFARE Ultralight EV1, MIFARE Ultralight C
  - MIFARE DESFire Light
  - NTAG DNA
  - ICODE DNA
  - UCODE DNA
- Secure storage and updating of keys
  - 128 key entries for symmetric cryptography
  - 3 RSA key entries for asymmetric cryptography
  - 8 ECC public key entries for signature verification
  - 4 ECC curves entries
  - 48 EMV CA public key entries (supports 8 RID minimum)
- SHA-1, SHA-224 and SHA-256 hashing computation
- TDEA and AES-based key diversification
- Generic cryptography commands for user-defined schemes
- Supports EMVCo terminal functionality
- True random number generator (TRNG) compliant to AIS-31

### 2.2 Communication

- ISO/IEC 7816 (part 2 and 3) contact interface
  - Support Class A, B and C operating condition
  - Support ISO/IEC 7816 baud rates
  - Support high-speed baud rates up to 1.5 Mbit/s
- Optional I2C slave mode host interface (only available on HVQFN package)
- Communication protocol compliant with ISO/IEC 7816-3 T=1 protocol
- Up to four logical channels; simultaneous multiple card support
- Support for MIFARE DESFire and MIFARE Plus authentication (with related secure messaging and session key generation)
- Secure Host to SAM and back end to SAM communication with symmetric cryptography including 3-pass authentication for confidentiality and integrity
- Secure Host to SAM and back end to SAM communication with RSA-based cryptography for key updating
- X-mode direct interface with NXP's contactless reader ICs (RC663, RC52x, PN512)

## 2.3 Programmable logic (restricted feature) <sup>2</sup>

- Up to 32 kB of code and data in EEPROM for user customized functionality
- 1 kB of RAM for user's dynamic data
- Internal Host access to all MIFARE SAM AV3 commands

## 2.4 Security evaluation and certification

- CC EAL6+ certified hardware platform (based on NXP's SmartMX2 P6022y VB)
- Composite certified with MIFARE Security Evaluation Scheme (Equivalent to EMVCo Security Evaluation)  
(Evaluation lab: TÜViT, Certification lab: UL)
- FIPS140-2 CAVP certified

## 2.5 New features

This section gives an overview of the new features compared to MIFARE SAM AV2. Please see [\[1\]](#) for details.

- All new features from MIFARE DESFire EV2 requiring cryptographic operations. This includes EV2 secure messaging and Transaction MAC support (incl CommitReaderID).
- All new features from MIFARE Plus EV1 requiring cryptographic operations. This includes EV1 secure messaging, Transaction MAC support (incl CommitReaderID) and Sector Security Level Switching.
- New Virtual Card Selection and Proximity Check protocols.
- Post-Delivery Configuration support.
- MIFARE Ultralight EV1 password authentication.
- AES authentication according to ISO/IEC 29167-10 for UCODE and ICODE support.
- LRP support for DESFire secure messaging, as supported by DESFire Light and NTAG42x(TT) and for Offline Crypto operations.
- ECC originality signature verification as supported by all recent MIFARE products.
- Generic CMAC-based key derivation for a.o. Transaction MAC session key generation and (e.g. UCODE) key diversification.
- Fine-grained key access control.
- EMV terminal support for certificate verification, offline authentication and pin code verification.
- Programmable Logic feature to allow customized business logic and a.o. key diversifications to be run within the SAM.
- Personalization SAM feature to generate cryptogram to export keys for injection in another SAM for AES variant and for RSA variant.
- AES-256 support for Offline Crypto and SAM-Host protection.
- RSA OAEP encryption and decryption.
- ATR configuration.
- I2C slave interface in addition to ISO/IEC 7816 interface (for HVQFN only).

<sup>2</sup> Note: The PL code uploading functionality is only available to a limited set of customers.

### 3 Ordering information

Table 1. Ordering information

| Type number        | Package |  |          |
|--------------------|---------|--|----------|
|                    | Name    | Description  | Version  |
| MF4SAM3X84/9BA6AU  | PCM1.5  | contact chip card module (super 35 mm tape format, 8 contact), minimum order quantity: 11.900  | SOT658-1 |
| MF4SAM3X84/9BA6AUS | PCM1.5  | contact chip card module (super 35 mm tape format, 8 contact), minimum order quantity: 1.000   | SOT658-1 |
| MF4SAM3HN/9BA6AU   | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm; reel pack; minimum order quantity: 6.000 | SOT617-3 |
| MF4SAM3U15/9BA6AU  | wafer   | 150 mm thickness sawn wafer on film frame carrier (FFC)  | NAU000   |

4 Block diagram

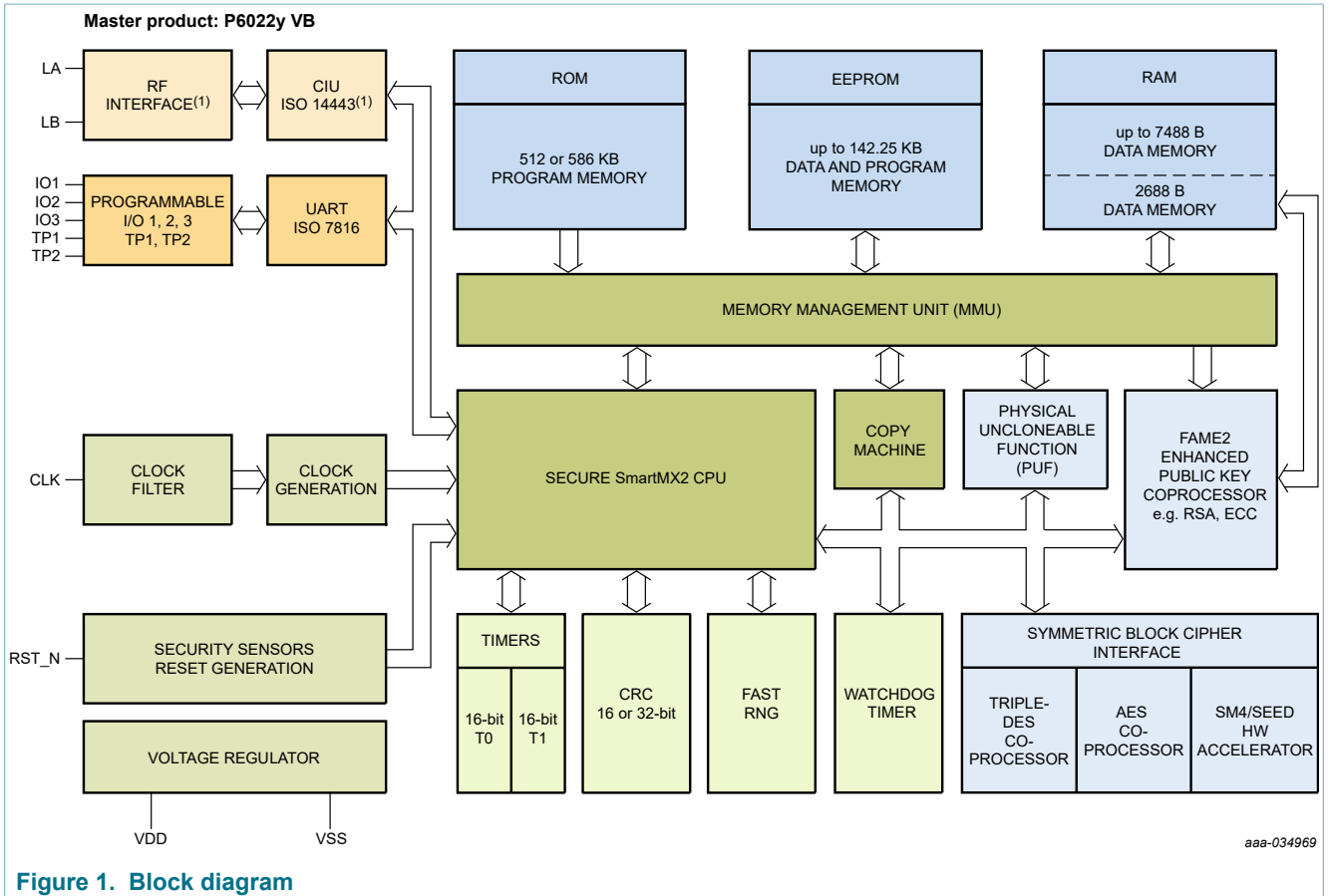


Figure 1. Block diagram

## 5 Pinning information

### 5.1 Pin description

#### 5.1.1 PCM1.5 pin configuration

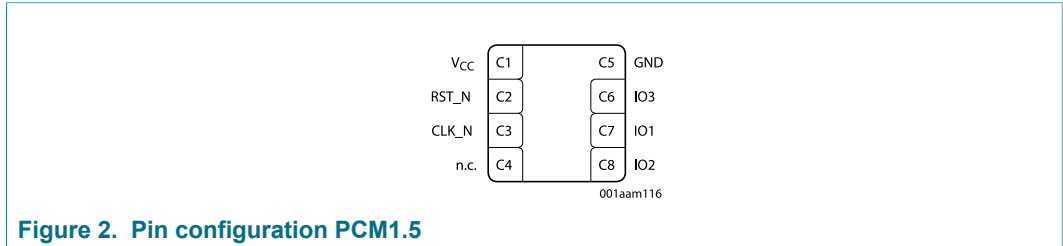
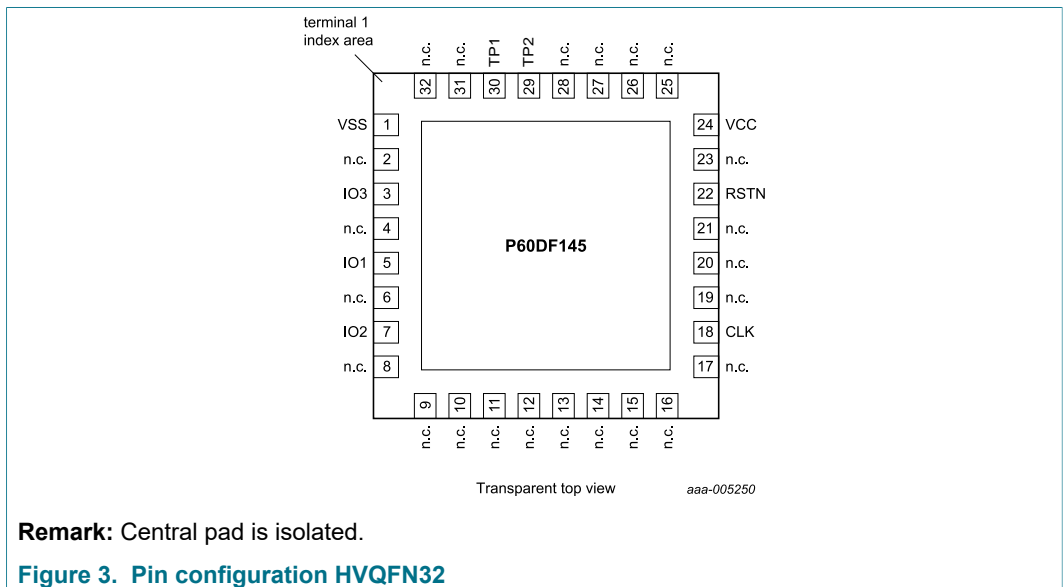


Figure 2. Pin configuration PCM1.5

Table 2. Pin description PCM 1.5 MIFARE SAM AV3

| ISO 7816 |          | MIFARE SAM AV3  |     |   |
|----------|----------|-----------------|-----|---|
| Pad      | Symbol   | Symbol          | Pad | Description                                       |
| C1       | VCC      | V <sub>CC</sub> | C1  | power supply voltage input                        |
| C2       | RST      | RST_N           | C2  | reset input, active LOW                           |
| C3       | CLK      | CLK_N           | C3  | clock input                                       |
| C4       | reserved | n.c.            | C4  | n.c.  |
| C5       | GND      | GND             | C5  | ground (reference voltage) input                  |
| C6       | VPP      | IO3             | C6  | used for I2C communication to RC (SCL)            |
| C7       | IO1      | IO1             | C7  | input/output for serial data (host communication) |
| C8       | reserved | IO2             | C8  | used for I2C communication to RC (SDA)            |

#### 5.1.2 HVQFN32 pin configuration



Remark: Central pad is isolated.

Figure 3. Pin configuration HVQFN32

Table 3. Pin description HVQFN32 MIFARE SAM AV3

| Pad | Symbol | Description  |
|-----|--------|--|
| 1   | GND    | ground (reference voltage) input   |
| 3   | IO3    | used for I2C communication to RC (SCL)   |
| 5   | IO1    | input/output for serial data (ISO7816 or SDA_Slave for I2C host communication)       |
| 7   | IO2    | used for I2C communication to RC (SDA)   |
| 24  | VCC    | power supply voltage input   |
| 22  | RST_N  | reset input, active LOW  |
| 18  | CLK_N  | clock input  |
| 29  | TP2    | SCL_Slave: used for I2C communication to Host when I2C host communication is enabled |
| 30  | TP1    | I2C_Enable: enable I2C host communication when high                                  |

## 6 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

| Symbol        | Parameter                             | Conditions                                     | Min            | Max            | Unit  |    |
|---------------|---------------------------------------|--|----------------|----------------|-------|----|
| $V_{DD(AMR)}$ | supply voltage                        |  | -0.5           | +6.0           | V     |    |
| $V_{I(AMR)}$  | input voltage                         | any signal pad                                 | -0.5           | $V_{DD} + 0.5$ | V     |    |
| $I_{I(AMR)}$  | input current                         | pads IO1, IO2, IO3 and TP1, TP2 <sup>[1]</sup> | -              | ± 15.0         | mA    |    |
| $I_O$         | output current                        | pads IO1, IO2, IO3 and TP1, TP2 <sup>[1]</sup> | -              | ± 15.0         | mA    |    |
| $I_{lu}$      | latch-up current                      | $V_I < 0$ V or $V_I > V_{DD}$                  | -              | ± 100          | mA    |    |
| $V_{esd}$     | electrostatic discharge voltage (HBM) | pads VDD, VSS, CLK, RST_N, IO1, IO2, IO3       | <sup>[2]</sup> | -              | ± 4.0 | kV |
|               |                                       | TP1, TP2                                       | <sup>[3]</sup> | -              | ± 2.0 | kV |
|               | electrostatic discharge voltage (CDM) | all pads                                       | <sup>[4]</sup> | -              | ± 500 | V  |
| $P_{tot}$     | Total power dissipation               |  | <sup>[5]</sup> | -              | 1     | W  |
| $T_{stg}$     | Storage temperature                   |  | <sup>[6]</sup> | -55            | 125   | °C |

[1] If IO2 and IO3 are available.

[2] In accordance with ANSI/ESDA/JEDEC JS-001-2011, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.

[3] Only available if enabled via OEF setting.

[4] In accordance with JEDEC JESD22-C101 for Charged-Device Model (CDM).

[5] Depending on appropriate thermal resistance of the package.

[6] Depending on delivery type, refer to *NXP Semiconductors General Specification for 12" Wafers* (15) and to *NXP Semiconductors Contact & Dual Interface Chip Card Module Specification* (16).

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.



## 7 Recommended operating conditions

Table 5. Operating conditions

| Symbol                | Parameter   | Conditions  | Min  | Typ | Max             | Unit |
|-----------------------|---|---|------|-----|-----------------|------|
| V <sub>DD</sub> (5.0) | Supply voltage <sup>[1]</sup>                           | Class A/5 V nominal supply voltage contact interface operation  | 4.5  | 5.0 | 5.5             | V    |
| V <sub>DD</sub> (3.0) |   | Class B/3 V nominal supply voltage contact interface operation  | 2.7  | 3.0 | 3.3             | V    |
| V <sub>DD</sub> (1.8) |   | Class C/1.8V nominal supply voltage contact interface operation | 1.62 | 1.8 | 1.98            | V    |
| V <sub>I</sub>        | DC input voltage on digital inputs and digital I/O pads | -   | 0    | -   | V <sub>DD</sub> | V    |
| T <sub>amb</sub>      | Operating ambient temperature <sup>[2]</sup>            |   | -25  | -   | +85             | °C   |

[1] All described supply voltages according to ISO/IEC 7816-3.

[2] All product properties and values specified within this data sheet are only valid within the operating ambient temperature range.

The supported operating supply voltage ranges limited by exception sensors covers the whole range of classes A, B and C. The Product Name devices operate within the full voltage range described in [Figure 4](#).

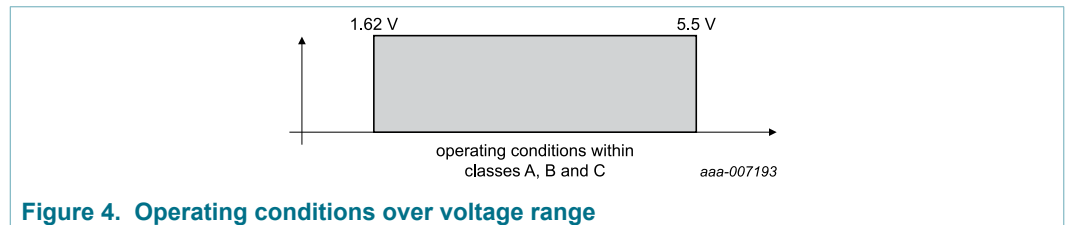


Figure 4. Operating conditions over voltage range

## 8 Static characteristics

### 8.1 Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the Smart Card IC are considered positive.

### 8.2 Levels and currents

**Table 6. Electrical DC characteristics of Input/Output: IO1, IO2 and IO3**

Conditions:  $V_{DD} = 1.62\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ , unless otherwise specified

| Symbol   | Parameter   | Conditions   | Min          | Typ | Max            | Unit          |
|----------|---|--|--------------|-----|----------------|---------------|
| $V_{IH}$ | HIGH level input voltage  |  | $0.7 V_{DD}$ | -   | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | LOW level input voltage   |  | -0.3         | -   | $0.25 V_{DD}$  | V             |
| $I_{IH}$ | HIGH level input current in "weak pull-up" input mode                     | $0.7 V_{DD} \leq V_I \leq V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{IH(max)}$ : $V_I = 0.7 V_{DD}$ , $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C     | 0            | -   | -20            | $\mu\text{A}$ |
| $I_{IL}$ | LOW level input current   | $0\text{ V} \leq V_I \leq 0.3 V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{IL(max)}$ : $V_I = 0\text{ V}$ , $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | -            | -   | -50            | $\mu\text{A}$ |
| $I_{TL}$ | HIGH-to-LOW transition input current (only in "quasi-bidirectional" mode) | $0.3 V_{DD} < V_I \leq V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$V_I = 0.5 V_{DD}$ , $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C                        | [1]          |     |                |               |
|          |   | Class A  | -            | -   | -300           | $\mu\text{A}$ |
|          |   | Class B  | -            | -   | -250           | $\mu\text{A}$ |
|          |   | Class C  | -            | -   | -200           | $\mu\text{A}$ |
| $I_I$    | Input current in "weak pull-up" input mode                                | $0\text{ V} \leq V_I \leq V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{I(max)}$ : $V_I = 0\text{ V}$ , $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C      | 0            | -   | -50            | $\mu\text{A}$ |

| Symbol             | Parameter  | Conditions   | Min | Typ                        | Max                         | Unit |
|--------------------|--|--|-----|----------------------------|-----------------------------|------|
| I <sub>ILIH</sub>  | Leakage input current at input voltage beyond V <sub>DD</sub> in "weak pull-up" input mode         | V <sub>DD</sub> < V <sub>I</sub> ≤ V <sub>DD</sub> + 0.3 V; -25 °C ≤ T <sub>amb</sub> ≤ +85 °C;<br>Test conditions: V <sub>I</sub> = V <sub>DD</sub> + 0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C | -   | -                          | 20                          | μA   |
| I <sub>ILIL</sub>  | Leakage input current at input voltage below V <sub>SS</sub> in "weak pull-up" input mode          | -0.3 V ≤ V <sub>I</sub> < 0 V; -25 °C ≤ T <sub>amb</sub> ≤ +30 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +30 °C  | -   | -                          | -50                         | μA   |
|                    |  | -0.3 V ≤ V <sub>I</sub> < 0 V; +30 °C < T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C  | -   | -                          | -275                        | μA   |
| I <sub>ILIHQ</sub> | Leakage input current at input voltage beyond V <sub>DD</sub> (only in "quasi-bidirectional" mode) | V <sub>DD</sub> < V <sub>I</sub> ≤ V <sub>DD</sub> + 0.3 V; -25 °C ≤ T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = V <sub>DD</sub> + 0.3 V; V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C     | -   | -                          | 100                         | μA   |
| I <sub>ILILQ</sub> | Leakage input current at input voltage below V <sub>SS</sub> (only in "quasi-bidirectional" mode)  | -0.3 V ≤ V <sub>I</sub> < 0 V; -25 °C ≤ T <sub>amb</sub> ≤ +30 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +30 °C  | -   | -                          | -75                         | μA   |
|                    |  | -0.3 V ≤ V <sub>I</sub> < 0 V; +30 °C < T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C  | -   | -                          | -300                        | μA   |
| V <sub>OH</sub>    | HIGH level output voltage  | I <sub>OH</sub> = -20 μA;<br>Class A condition   | [2] | 3.8<br>0.7 V <sub>DD</sub> | -                           | V    |
|                    |  | I <sub>OH</sub> = -20 μA;<br>Class B or C condition  | [2] | 0.7 V <sub>DD</sub>        | -                           | V    |
| V <sub>OL</sub>    | LOW level output voltage   | Class A or B condition;<br>I <sub>OL</sub> = 1.0 mA  | -   | -                          | 0.3                         | V    |
|                    |  | Class C condition;<br>I <sub>OL</sub> = 1.0 mA<br>I <sub>OL</sub> = 0.5 mA   | -   | -                          | 0.3<br>0.15 V <sub>DD</sub> | V    |

- [1] IO1, IO2 and IO3 source a transition current when being externally driven from HIGH to LOW. This transition current ( $I_{TL}$ ) reaches its maximum value when the input voltage  $V_I$  is approximately  $0.5 V_{DD}$ . Input current  $I_{TL}$  is tested at input voltage  $V_I = 0.5 V_{DD}$ . Current  $I_{IL}$  is tested at input voltage  $V_I = 0.3 V$ . [Figure 5](#) shows the input characteristic of this quasi-bidirectional port mode.
- [2] External pull-up resistor  $20\text{ k}\Omega$  to  $V_{DD}$  assumed. The worst case test condition for parameter  $V_{OH}$  is present at minimum  $V_{DD}$ . For class A supply voltage conditions  $V_{DD} = 4.5\text{ V}$  is the worst case with respect to the fix specification limit  $V_{OHmin} = 3.8\text{ V}$  ( $0.844 V_{DD}$ ). The supply voltage related limit " $0.7 V_{DD}$ " is a stricter requirement than the fix value  $3.8\text{ V}$  at high  $V_{DD}$  values ( $0.7 V_{DD} = 3.85\text{ V}$  at  $V_{DD} = 5.5\text{ V}$ ). So, in the  $V_{DD}$  range  $4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{OHmin}$  is specified as "the larger value of  $0.7 V_{DD}$  and  $3.8\text{ V}$ , respectively". The  $V_{OHmin}$  value ( $0.7 V_{DD}$ ) cannot be guaranteed in "quasi-bidirectional" mode at an output current of  $I_{OH} = -20\text{ }\mu\text{A}$  - the strong output drive mode must be used.

**Table 7. Electrical DC characteristics of Inputs CLK and RST\_N<sup>[1][2]</sup>**

Conditions:  $V_{DD} = 1.62\text{ V}$  to  $5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ , unless otherwise specified

| Symbol  | Parameter  | Conditions   | Min          | Typ | Max            | Unit          |
|---|--|--|--------------|-----|----------------|---------------|
| <b>Inputs CLK (when the IC is not in reset) and RST_N</b> |  |  |              |     |                |               |
| $V_{IH1}$   | HIGH level input voltage                               |  | $0.7 V_{DD}$ | -   | $V_{DD} + 0.3$ | V             |
| $V_{IL1}$   | LOW level input voltage                                |  | -0.3         | -   | $0.25 V_{DD}$  | V             |
| $I_{IH1}$   | HIGH level input current (weak pull-down is on)        | $0.7 V_{DD} \leq V_I \leq V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{IH1(max)}$ : $V_I = V_{DD}$ ,<br>$V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C   | -            | -   | 20             | $\mu\text{A}$ |
| $I_{IL1}$   | LOW level input current (weak pull-down is on)         | $0\text{ V} \leq V_I \leq 0.3 V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{IL1(max)}$ : $V_I = 0.3 V_{DD}$ ,<br>$V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C   | 0            | -   | 20             | $\mu\text{A}$ |
| $I_{I1}$  | Input current (weak pull-down is on)                   | $0\text{ V} \leq V_I \leq V_{DD}$ ;<br>Test conditions for the maximum absolute value:<br>$I_{I1(max)}$ : $V_I = V_{DD}$ ,<br>$V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C  | 0            | -   | 20             | $\mu\text{A}$ |
| $I_{ILIH1}$   | Leakage input current at input voltage beyond $V_{DD}$ | $V_{DD} < V_I \leq V_{DD} + 0.3\text{ V}$ ; $-25\text{ }^\circ\text{C} \leq T_{amb} \leq +85\text{ }^\circ\text{C}$<br>Test conditions: $V_I = V_{DD} + 0.3\text{ V}$ ;<br>$V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C;<br>$T_{amb} = +85\text{ }^\circ\text{C}$ | -            | -   | 20             | $\mu\text{A}$ |
| $I_{ILIL1}$   | Leakage input current at input voltage below $V_{SS}$  | $-0.3\text{ V} \leq V_I < 0\text{ V}$ ; $-25\text{ }^\circ\text{C} \leq T_{amb} \leq +30\text{ }^\circ\text{C}$<br>Test conditions: $V_I = -0.3\text{ V}$ ;<br>$V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C;<br>$T_{amb} = +30\text{ }^\circ\text{C}$             | -            | -   | -50            | $\mu\text{A}$ |

| Symbol                             | Parameter   | Conditions  | Min                 | Typ | Max                   | Unit |
|------------------------------------|---|---|---------------------|-----|-----------------------|------|
|                                    |   | -0.3 V ≤ V <sub>I</sub> < 0 V; +30 °C < T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C   | -                   | -   | -200                  | μA   |
| <b>Input CLK (during IC reset)</b> |   |   |                     |     |                       |      |
| V <sub>IH2</sub>                   | HIGH level input voltage                                      |   | 0.7 V <sub>DD</sub> | -   | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL2</sub>                   | LOW level input voltage                                       |   | -0.3                | -   | 0.25 V <sub>DD</sub>  | V    |
| I <sub>IH2</sub>                   | HIGH level input current (weak pull-up is on)                 | 0.7 V <sub>DD</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub> ;<br>Test conditions for the maximum absolute value:<br>I <sub>IH2(max)</sub> : V <sub>I</sub> = 0.7 V <sub>DD</sub> ,<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C              | 0                   | -   | -20                   | μA   |
| I <sub>IL2</sub>                   | HIGH level input current (weak pull-up is on)                 | 0 V ≤ V <sub>I</sub> ≤ 0.3 V <sub>DD</sub> ;<br>Test conditions for the maximum absolute value:<br>I <sub>IL2(max)</sub> : V <sub>I</sub> = 0V,<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C  | -                   | -   | -20                   | μA   |
| I <sub>I2</sub>                    | Input current (weak pull-up is on)                            | 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub> ;<br>Test conditions for the maximum absolute value:<br>I <sub>I2(max)</sub> : V <sub>I</sub> = 0 V,<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C  | 0                   | -   | -20                   | μA   |
| I <sub>LIH2</sub>                  | Leakage input current at input voltage beyond V <sub>DD</sub> | V <sub>DD</sub> < V <sub>I</sub> ≤ V <sub>DD</sub> + 0.3 V; -25 °C ≤ T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = V <sub>DD</sub> + 0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C | -                   | -   | 20                    | μA   |
| I <sub>LIL2</sub>                  | Leakage input current at input voltage below V <sub>SS</sub>  | -0.3 V ≤ V <sub>I</sub> < 0 V; -25 °C ≤ T <sub>amb</sub> ≤ +30 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +30 °C   | -                   | -   | -50                   | μA   |
|                                    |   | -0.3 V ≤ V <sub>I</sub> < 0 V; +30 °C < T <sub>amb</sub> ≤ +85 °C<br>Test conditions: V <sub>I</sub> = -0.3 V;<br>V <sub>DD</sub> = V <sub>DD(max)</sub> of the respective supply voltage class A, B or C;<br>T <sub>amb</sub> = +85 °C   | -                   | -   | -200                  | μA   |

- [1] The active low RST\_N input and outside reset state also the CLK input internally activate a resistive pull-down device to VSS. Accordingly a current is flowing into the pad at voltages above 0 V. [Figure 7](#) shows this input characteristic. In CLOCKSTOP mode the preferred electrical state on CLK is a LOW level, in order to minimize the power consumption.
- [2] The CLK input internally has a resistive pull-up device to VDD activated during IC reset. Accordingly a current is flowing out of the pad at voltages below VDD. [Figure 8](#) shows this input characteristic.

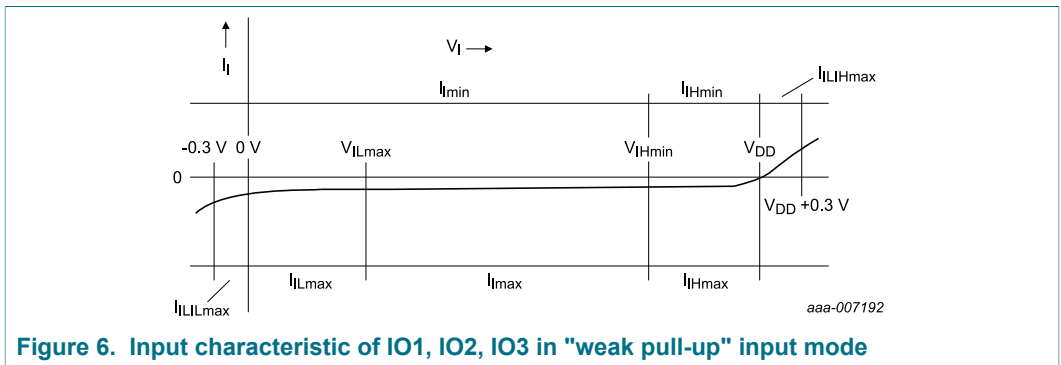
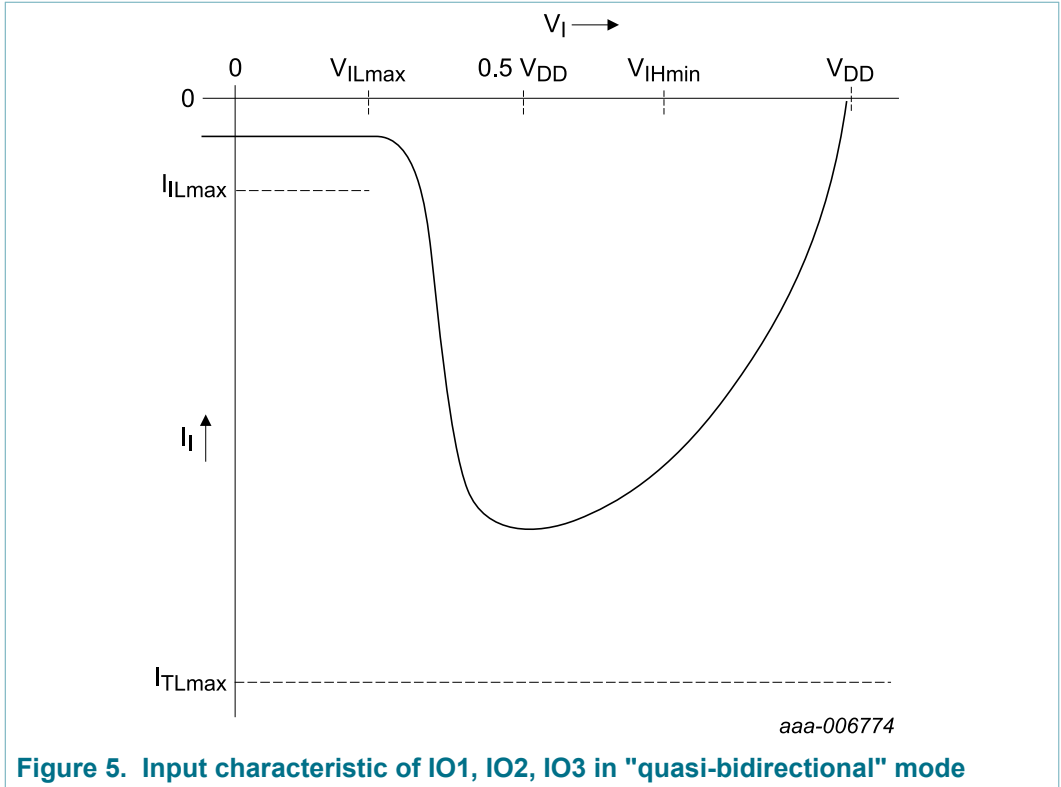
**Table 8. Electrical DC characteristics of TP1 and TP2**

Conditions: (A)  $V_{DD} = 1.62$  to  $1.98$  V;  $V_{DDAE} = V_{DD}$ ;

(B)  $V_{DD} = 2.2$  to  $5.5$  V (i.e. outside Class C supply range);  $V_{DDAE(NOM)} = 1.8$  V;

$V_{SS} = 0$  V;  $T_{amb} = -25$  °C to  $+85$  °C, unless otherwise specified

| Symbol      | Parameter  | Conditions   | Min              | Typ | Max              | Unit    |
|-------------|--|--|------------------|-----|------------------|---------|
| $V_{IHT}$   | HIGH level input voltage   |  | $0.7 V_{DDAE}$   | -   | $V_{DDAE} + 0.3$ | V       |
| $V_{ILT}$   | LOW level input voltage  |  | -0.3             | -   | $0.25 V_{DDAE}$  | V       |
| $I_{IHD}$   | HIGH level input current maximum (resistive pull-down is on)                         | $0.7 V_{DDAE} \leq V_I \leq V_{DDAE}$ ;<br>Test conditions for the maximum absolute value:<br>$V_I = V_{DDAE}$ ;<br>$V_{DDAE} = V_{DDAE(max)}$ ;<br>for the minium absolute value:<br>$V_I = 0.7 V_{DDAE}$ ;<br>$V_{DDAE} = V_{DDAE(min)}$ | 10               | -   | 100              | $\mu$ A |
| $I_{ILD}$   | LOW level input current maximum (resistive pull-down is on)                          | $0 V \leq V_I \leq 0.3 V_{DDAE}$ ;<br>Test conditions for the maximum absolute value:<br>$V_I = 0.3 V_{DDAE}$ ;<br>$V_{DDAE} = V_{DDAE(max)}$ ;  | 0                | -   | 20               | $\mu$ A |
| $I_{ILIH3}$ | Leakage input current at input voltage beyond $V_{DDAE}$ (resistive pull-down is on) | $V_{DDAE} < V_I \leq V_{DDAE} + 0.3$ V;<br>$-25$ °C $\leq T_{amb} \leq +85$ °C;<br>Test conditions:<br>$V_I = 2.3$ V;<br>$T_{amb} = +85$ °C  | -                | -   | 150              | $\mu$ A |
| $I_{ILIL3}$ | Leakage input current at input voltage beyond $V_{SS}$ (resistive pull-down is on)   | $-0.3 V \leq V_I < 0$ V;<br>$-25$ °C $\leq T_{amb} \leq +30$ °C;<br>Test conditions:<br>$V_I = -0.3$ V;<br>$T_{amb} = +30$ °C  | 0                | -   | -150             | $\mu$ A |
|             |  | $-0.3 V \leq V_I < 0$ V;<br>$+30$ °C $< T_{amb} \leq +85$ °C;<br>Test conditions:<br>$V_I = -0.3$ V;<br>$T_{amb} = +85$ °C   | -                | -   | -300             | $\mu$ A |
| $V_{OH2}$   | HIGH level output voltage  | $I_{OH2} = -0.1$ $\mu$ A   | $V_{DDAE} - 0.3$ | -   | -                | V       |
| $V_{OL2}$   | LOW level output voltage   | $I_{OL2} = 1.2$ $\mu$ A  | -                | -   | 0.3              | V       |



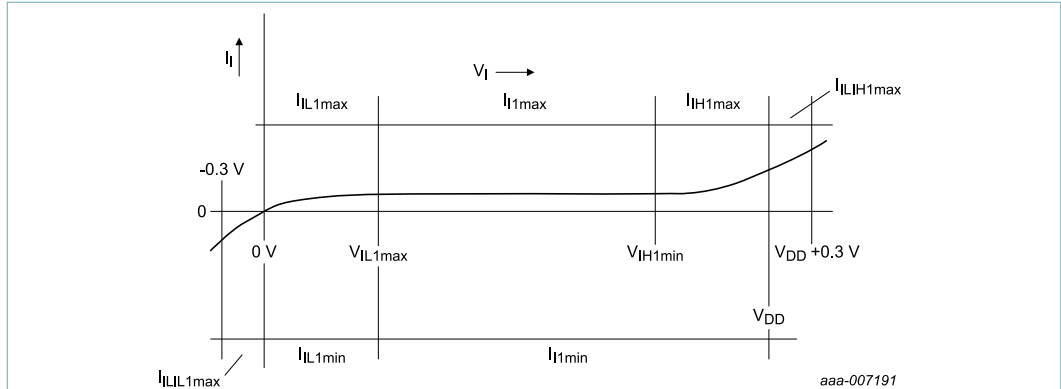


Figure 7. Input characteristic of CLK when the IC is not in reset and of RST\_N

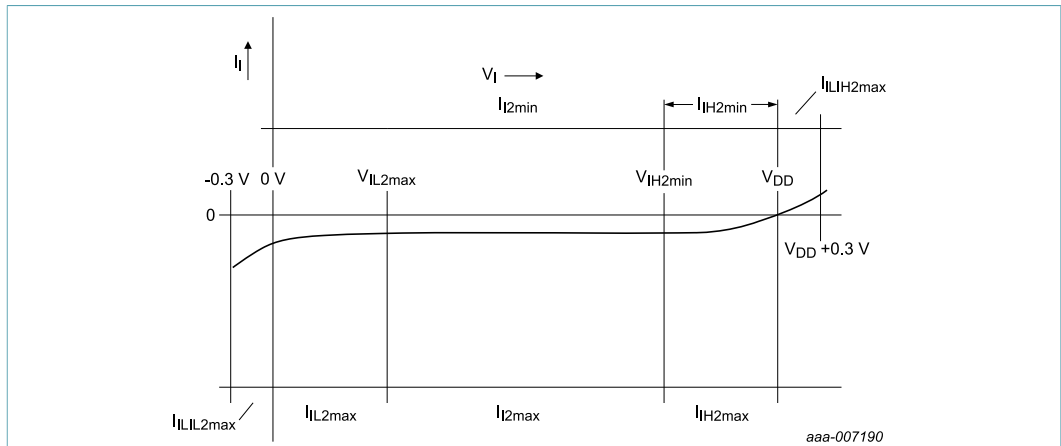


Figure 8. Input characteristic of CLK during IC reset

8.3 General and ISO/IEC 7816 I/O interface at ISO/IEC 7816-3: A/5 V, class B/3 V or class C/1.8 V class operation

Table 9. Electrical characteristics of IC supply current<sup>[1]</sup>

Conditions:  $V_{DD} = 1.62\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ , unless otherwise specified

| Symbol                      | Parameter                     | Conditions                              | Supply voltage class | Min  | Typ  | Max  | Unit |
|-----------------------------|-------------------------------|---|----------------------|------|------|------|------|
| <b>Supply</b>               |                               |   |                      |      |      |      |      |
| $V_{DD}$                    | supply voltage range          | Class A: 5 V range                      | A (5 V)              | 4.50 | 5.00 | 5.50 | V    |
|                             |                               | Class B: 3 V range                      | B (3 V)              | 2.70 | 3.00 | 3.30 | V    |
|                             |                               | Class C: 1.8 V range                    | C (1.8 V)            | 1.62 | 1.80 | 1.98 | V    |
| operating mode: Reset State |                               |   |                      |      |      |      |      |
| $I_{DD}$                    | supply current operating mode | $f_{CLK} = 10\text{ MHz}$ , RESET state | A (5 V)              | -    | 1.20 | 4.00 | mA   |
|                             |                               |   | B (3 V)<br>C (1.8 V) |      |      |      |      |
| operating mode: typical CPU |                               |   |                      |      |      |      |      |



| Symbol        | Parameter  | Conditions   | Supply voltage class            | Min | Typ              | Max    | Unit          |
|---------------|--|--|---------------------------------|-----|------------------|--------|---------------|
|               | no coprocessor active  | $f_{CLK} = 10 \text{ MHz}$ , CPU at $f_{CLK}$  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 1.60             | 4.00   | mA            |
|               | no coprocessor active  | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU in free running mode   | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 2.50             | 4.00   | mA            |
|               | DES coprocessor active<br>(DES int. 32 MHz)  | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 4.00             | 6.00   | mA            |
|               | DES coprocessor active<br>(DES int. 96 MHz)  | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 8.60             | 10.50  | mA            |
|               | AES coprocessor active<br>(AES int. 32 MHz)  | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 3.10             | 5.00   | mA            |
|               | AES coprocessor active<br>(AES int. 96 MHz)  | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 5.60             | 8.00   | mA            |
|               | Fame2 coprocessor active<br>(Fame2 clock = 16 MHz,<br>double multiplier mode)                            | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 3.90             | 6.50   | mA            |
|               | Fame2 coprocessor active<br>(Fame2 clock = 48 MHz,<br>double multiplier mode)                            | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 5.40             | 8.50   | mA            |
|               | Fame2 coprocessor active<br>(Fame2 clock = free<br>running, double multiplier<br>mode)                   | $f_{CLK} = 10 \text{ MHz}$ ,<br>CPU at int. 4 MHz  | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 5.40             | 10.50  | mA            |
| $I_{DD(ID)}$  | supply current CPU<br>IDLE mode (this parameter<br>should not be mixed-up<br>with the ETSI "idle state") | $f_{CLK} = 10 \text{ MHz}$ , $T_{amb} = 25 \text{ }^\circ\text{C}$   | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 0.80             | 1.50   | mA            |
| $I_{DD(SLP)}$ | supply current SLEEP<br>mode (this parameter<br>should not be mixed-up<br>with the ETSI "idle state")    | $f_{CLK} = 10 \text{ MHz}$ , $T_{amb} = 25 \text{ }^\circ\text{C}$<br>(VDDCO power domain<br>switched off)   | A (5 V)<br>B (3 V)<br>C (1.8 V) | -   | 175.00<br>150.00 | 200.00 | $\mu\text{A}$ |
| $I_{DD(PD)}$  | supply current<br>CLOCKSTOP mode   | $V_{DDmin} \leq V_{DD} \leq V_{DDmax}$ ; Clock<br>to input CLK stopped, $T_{amb} = 25 \text{ }^\circ\text{C}$<br>(VDDCO power domain and<br>CLIF switched off) | A (5 V)                         | -   | 80.00            | 200.00 | $\mu\text{A}$ |
|               |  |  | B (3 V)<br>C (1.8 V)            | -   | 60.00            | 100.00 | $\mu\text{A}$ |

[1] Typical values are only referenced for information. They are subject to change without notice.

## 9 Dynamic characteristics

**Remark:** The P6022y VB only supports one single IO1.

### 9.1 General, ISO/IEC 7816 I/O and ISO/IEC 14443 I/O interfaces

**Table 10. Electrical AC characteristics of IO1, IO2, IO3, CLK and RST\_N**

Conditions:  $V_{DD} = 1.62\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ °C to }+85\text{ °C}$ , unless otherwise specified

| Symbol                                   | Parameter  | Conditions  |     | Min  | Typ <sup>[1]</sup> | Max                             | Unit |
|--|--|---|-----|------|--------------------|---------------------------------|------|
| <b>Input/Output: IO1, IO2 and IO3</b>    |  |   |     |      |                    |                                 |      |
| tr <sub>IO</sub>                         | I/O Input rise time  | Input/reception mode  | [2] | -    | -                  | 1                               | µs   |
|  |  |   | [3] | -    | -                  | 0.25 ×<br>t <sub>IOWx_min</sub> | µs   |
| tf <sub>IO</sub>                         | I/O Input fall time  | Input/reception mode  | [2] | -    | -                  | 1                               | µs   |
|  |  |   | [3] | -    | -                  | 0.25 ×<br>t <sub>IOWx_min</sub> | µs   |
| tr <sub>OIO</sub>                        | I/O Output rise time   | Output/transmission mode; C <sub>L</sub> = 30 pF                                |     | -    | -                  | 0.1                             | µs   |
| tf <sub>OIO</sub>                        | I/O Output fall time   | Output/transmission mode; C <sub>L</sub> = 30 pF                                |     | -    | -                  | 0.1                             | µs   |
| <b>Inputs: CLK and RST_N</b>             |  |   |     |      |                    |                                 |      |
| f <sub>CLK</sub>                         | External clock frequency in ISO/IEC 7816 UART applications               | t <sub>CLKW</sub> , T <sub>amb</sub> and V <sub>DD</sub> in their spec'd limits | [4] | 0.85 | -                  | 11.5                            | MHz  |
| t <sub>CLKW</sub>                        | Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK) |   | [5] | 40   | -                  | 60                              | %    |
| tr <sub>CLK</sub>                        | CLK input rise time  |   | [6] | -    | -                  | see [6]                         |      |
| tf <sub>CLK</sub>                        | CLK input fall time  |   | [6] | -    | -                  | see [6]                         |      |
| tr <sub>RST</sub>                        | RST_N input rise time  |   | [7] | -    | -                  | 400                             | µs   |
| tf <sub>RST</sub>                        | RST_N input fall time  |   | [7] | -    | -                  | 400                             | µs   |
| t <sub>RW</sub>                          | Reset pulse width (RST_N low)  |   |     | 40   | -                  | -                               | µs   |
| t <sub>WKP</sub>                         | Wake-up time from SLEEP mode   | f <sub>CLKmin</sub> ≤ f <sub>CLK</sub> ≤ f <sub>CLKmax</sub>                    |     | -    | 17                 | 20                              | µs   |
| t <sub>WKPIO</sub>                       | I/Ox LOW time for wake-up from SLEEP mode                                | level triggered ext.int.  |     | -    | 20                 | -                               | µs   |
|  |  | edge triggered ext.int.   |     | -    | 20                 | -                               | µs   |
| t <sub>WKPRST</sub>                      | RST_N LOW time for wake-up from SLEEP mode                               |   |     | 40   | -                  | -                               | µs   |
| <b>Inputs: CLK, RST_N, IO1, IO2, IO3</b> |  |   |     |      |                    |                                 |      |
| C <sub>PIN</sub>                         | Pin capacitances CLK, RST_N, IO1, IO2, IO3                               | Test frequency = 1 MHz; T <sub>amb</sub> = 25 °C                                |     | -    | -                  | 10                              | pF   |

[1] Typical values are only referenced for information. They are subject to change without notice.

- [2] At minimum IOx input signal HIGH or LOW level voltage pulse width of 3.2  $\mu$ s. This timing specification applies to ISO7816 configurations down to a minimum etu duration of 16 CLK cycles at a maximum CLK frequency of 5 MHz (TA1=0x96, (Fi/Di)=(512/32)), for example.
- [3] At minimum IOx input signal HIGH or LOW level voltage pulse width of less than 3.2  $\mu$ s. This timing specification applies to ISO7816 configurations beyond the conditions listed in note [2], down to a minimum etu duration of 8 CLK cycles at a maximum CLK frequency of 5 MHz (TA1=0x97, (Fi/Di)=(512/64)), for example. An 8 CLKs/etu @ fclk = 5 MHz configuration results in  $t_{IOWx\_min} = 1.6 \mu$ s, and in a time of 400 ns for  $t_{rIO\_max}$  and  $t_{fIO\_max}$ , matching the (Fi/Di)=(512/64) speed enhancement requirements of ETSI TS 102 221.
- [4] ISO/IEC 7816 I/O applications have to supply a clock signal to input CLK in the frequency range of 1 MHz to 10 MHz nominal. A  $\pm 15\%$  tolerance range yields the allowed limits of 0.85 MHz and 11.5 MHz.
- [5] During AC testing the inputs CLK, RST\_N, IO1, IO2 and IO3 are driven at 0 V to +0.3 V for a LOW input level and at  $V_{DD} - 0.3$  V to  $V_{DD}$  for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of  $V_{DD}$  (see Figure 9).
- [6] The maximum CLK rise and fall time is 10% of the CLK period  $1/f_{CLK}$  - with the following exception: In the CLK frequency range of 1 MHz to 5 MHz the maximum allowed CLK rise and fall time is 50 ns, if 10% of the CLK period is shorter than 50 ns.
- [7] The ETSI TS102 221/GSM 11.1x specifications specify a maximum reset signal (RST\_N) rise time and fall time of 400,000  $\mu$ s, respectively.

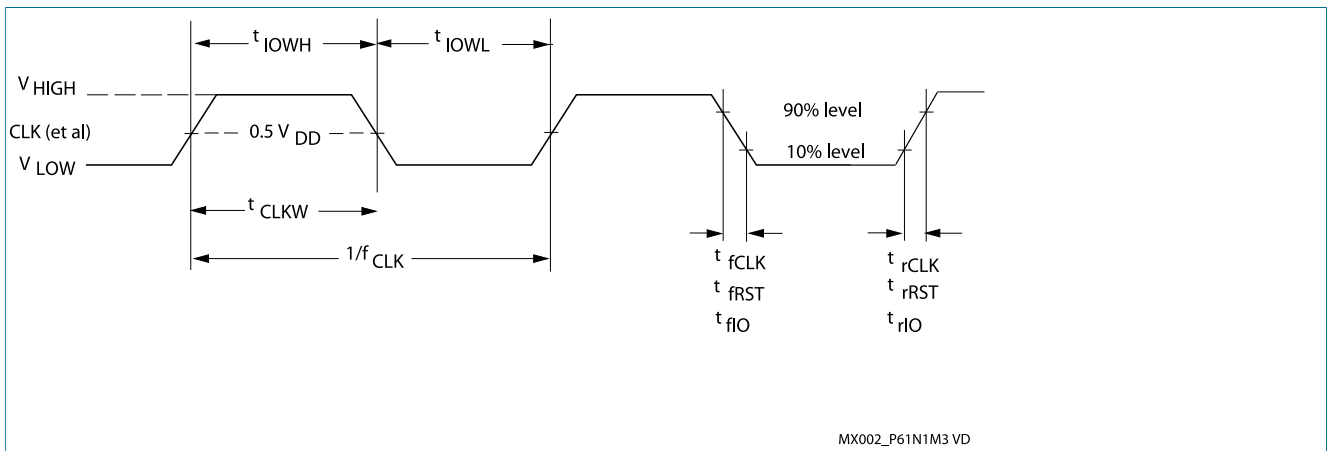


Figure 9. External clock drive and AC test timing reference points of CLK, RST\_N, IO1, IO2 and IO3 (see [1] and [2])

- [1] During AC testing the inputs CLK, RST\_N, IO1, IO2 and IO3 are driven at 0 V to +0.3 V for a LOW input level and at  $V_{DD} - 0.3$  V to  $V_{DD}$  for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of  $V_{DD}$ .
- [2]  $t_r$  is defined as rise time between 10% and 90% of the signal amplitude.  
 $t_f$  is defined as fall time between 90% and 10% of the signal amplitude.

Table 11. Electrical AC characteristics of TP1 and TP2

Conditions: (A)  $V_{DD} = 1.62$  to  $1.98$  V;  $V_{DDAE} = V_{DD}$ ; (B)  $V_{DD} = 2.2$  to  $5.5$  V (i.e. outside Class C supply range):  $V_{DDAE}(nom) = 1.8$  V;  $V_{SS} = 0$  V;  $T_{amb} = -25$  °C to  $+85$  °C, unless otherwise specified

| Symbol     | Parameter                    | Conditions                                    | Min | Typ | Max | Unit    |
|------------|------------------------------|---|-----|-----|-----|---------|
| $t_{rTP}$  | TP input rise time           | Input/reception mode                          | -   | -   | 1   | $\mu$ s |
| $t_{fTP}$  | TP input fall time           | Input/reception mode                          | -   | -   | 1   | $\mu$ s |
| $t_{rOTP}$ | TP output rise time          | Output/transmission mode;<br>$C_L = 30$ pF    | -   | -   | 50  | ns      |
| $t_{fOTP}$ | TP output fall time          | Output/transmission mode;<br>$C_L = 30$ pF    | -   | -   | 50  | ns      |
| $C_{iTP}$  | Pin characteristics TP1, TP2 | Test frequency = 1 MHz;<br>$T_{amb} = -25$ °C | -   | -   | 15  | pF      |

## 9.2 Non-Volatile memory

**Table 12. Non-volatile memory characteristics**

Conditions:  $V_{DD} = 1.62\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ °C to }+85\text{ °C}$ , unless otherwise specified

| Symbol     | Parameter   | Conditions                | Min              | Typ <sup>[1]</sup> | Max | Unit   |
|------------|---|---------------------------|------------------|--------------------|-----|--------|
| $t_{EEP}$  | EEPROM erase/program time   | [2]                       | -                | 2.00               | -   | ms     |
| $t_{EEE}$  | EEPROM erase time   |                           | -                | 1.25               | -   | ms     |
| $t_{EEW}$  | EEPROM program time   |                           | -                | 0.75               | -   | ms     |
| $t_{EER}$  | EEPROM data retention time  | $T_{amb} = +55\text{ °C}$ | 25               | -                  | -   | years  |
| $N_{EEC}$  | EEPROM endurance (number of programming cycles)   |                           | $5 \times 10^5$  | -                  | -   | cycles |
| $N_{EECM}$ | EEPROM endurance (maximum number of programming cycles applied to the whole memory block) |                           | $20 \times 10^6$ | $100 \times 10^6$  | -   | cycles |

[1] Typical values are only referenced for information. They are subject to change without notice.

[2] Given value specifies physical access times of EEPROM memory only.

## 9.3 I<sup>2</sup>C Slave interface bus timing

**Table 13. Non-volatile memory characteristics**

Conditions:  $V_{DD} = 1.62\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -25\text{ °C to }+85\text{ °C}$ , unless otherwise specified

| Symbol       | Parameter  | Conditions  | Min  | Max  | Unit |
|--------------|--|---|------|------|------|
| $f_{SCL}$    | SCL clock frequency                              |   | 0    | 350  | kHz  |
| $t_{HD,STA}$ | hold time (repeated) START condition             | after this period, the first clock pulse is generated | 4000 | -    | ns   |
| $t_{SU,STA}$ | set-up time for a repeated START condition       |   | 4700 | -    | ns   |
| $t_{SU,STO}$ | set-up time for STOP condition                   |   | 4000 | -    | ns   |
| $t_{LOW}$    | LOW period of the SCL clock                      |   | 4700 | -    | ns   |
| $t_{HIGH}$   | HIGH period of the SCL clock                     |   | 4000 | -    | ns   |
| $t_{HD,DAT}$ | data hold time                                   |   | 300  | 3450 | ns   |
| $t_{SU,DAT}$ | data set-up time                                 |   | 250  | -    | ns   |
| $t_{VD,DAT}$ | data valid time                                  |   | -    | 3450 | ns   |
| $t_{VD,ACK}$ | data valid acknowledge                           |   | -    | 3450 | ns   |
| $t_r$        | rise time  | SDA and SCL signals                                   | -    | 1000 | ns   |
| $t_f$        | fall time  | SDA and SCL signals                                   | -    | 300  | ns   |
| $t_{BUF}$    | bus free time between a STOP and START condition |   | 4700 | -    | ns   |

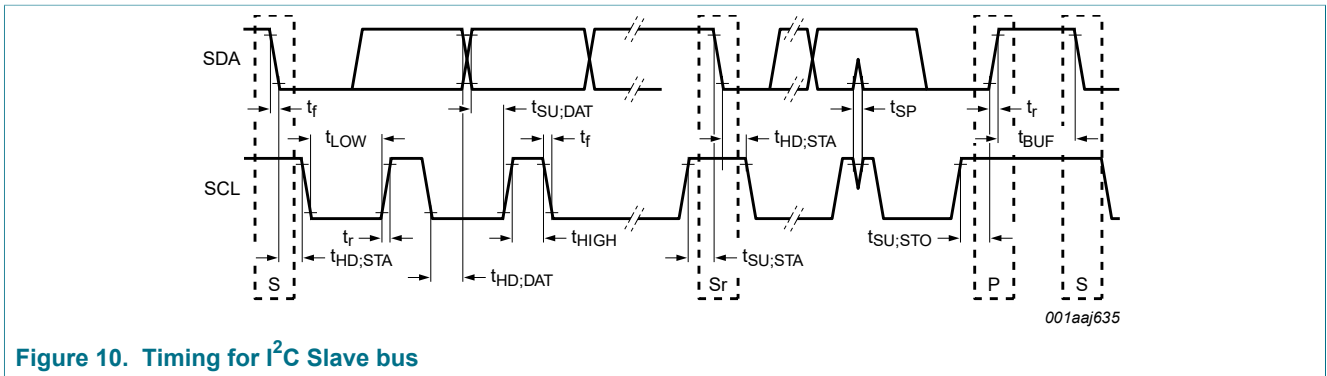


Figure 10. Timing for I<sup>2</sup>C Slave bus

10 Package outline

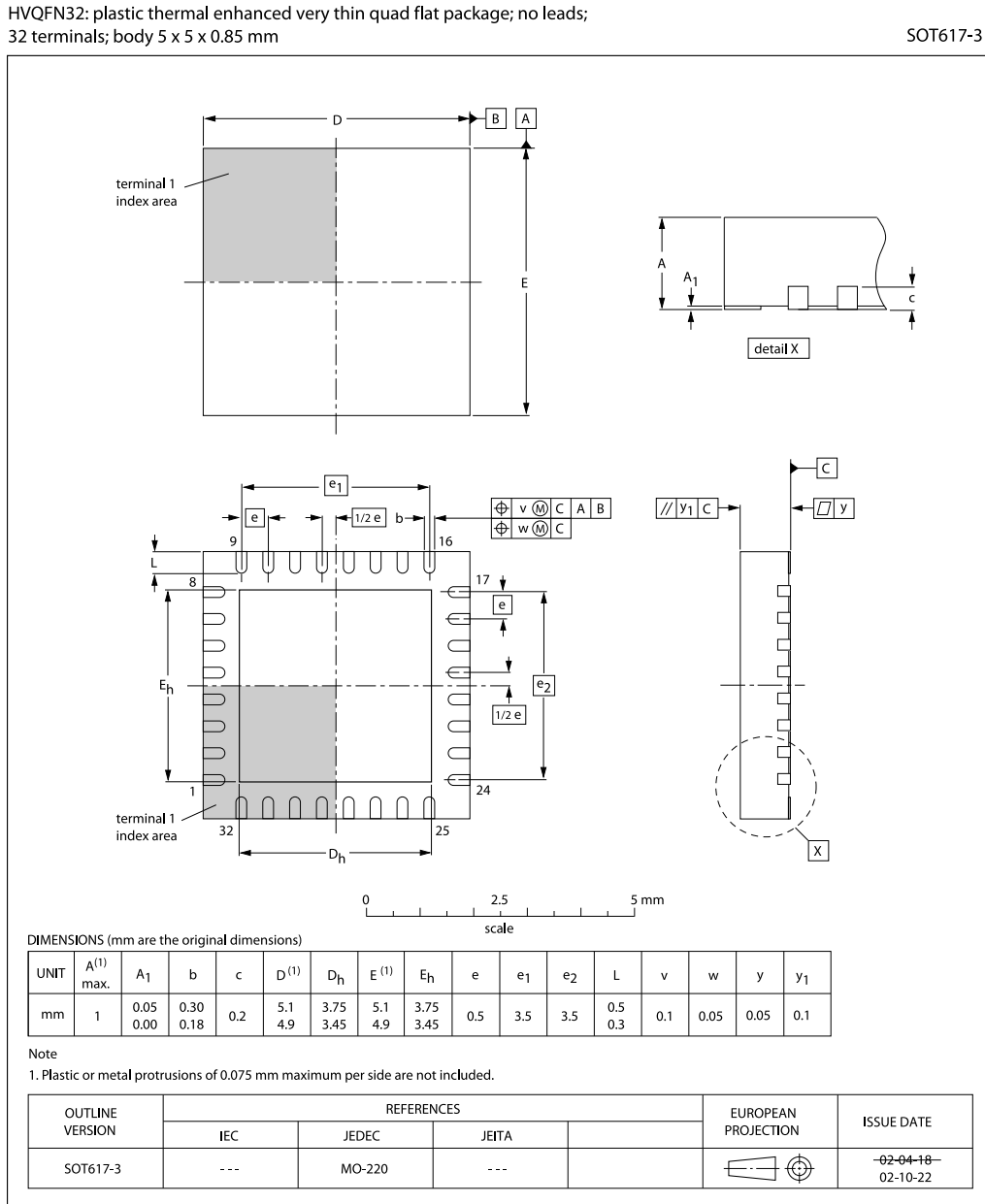


Figure 11. Package outline SOT617-3

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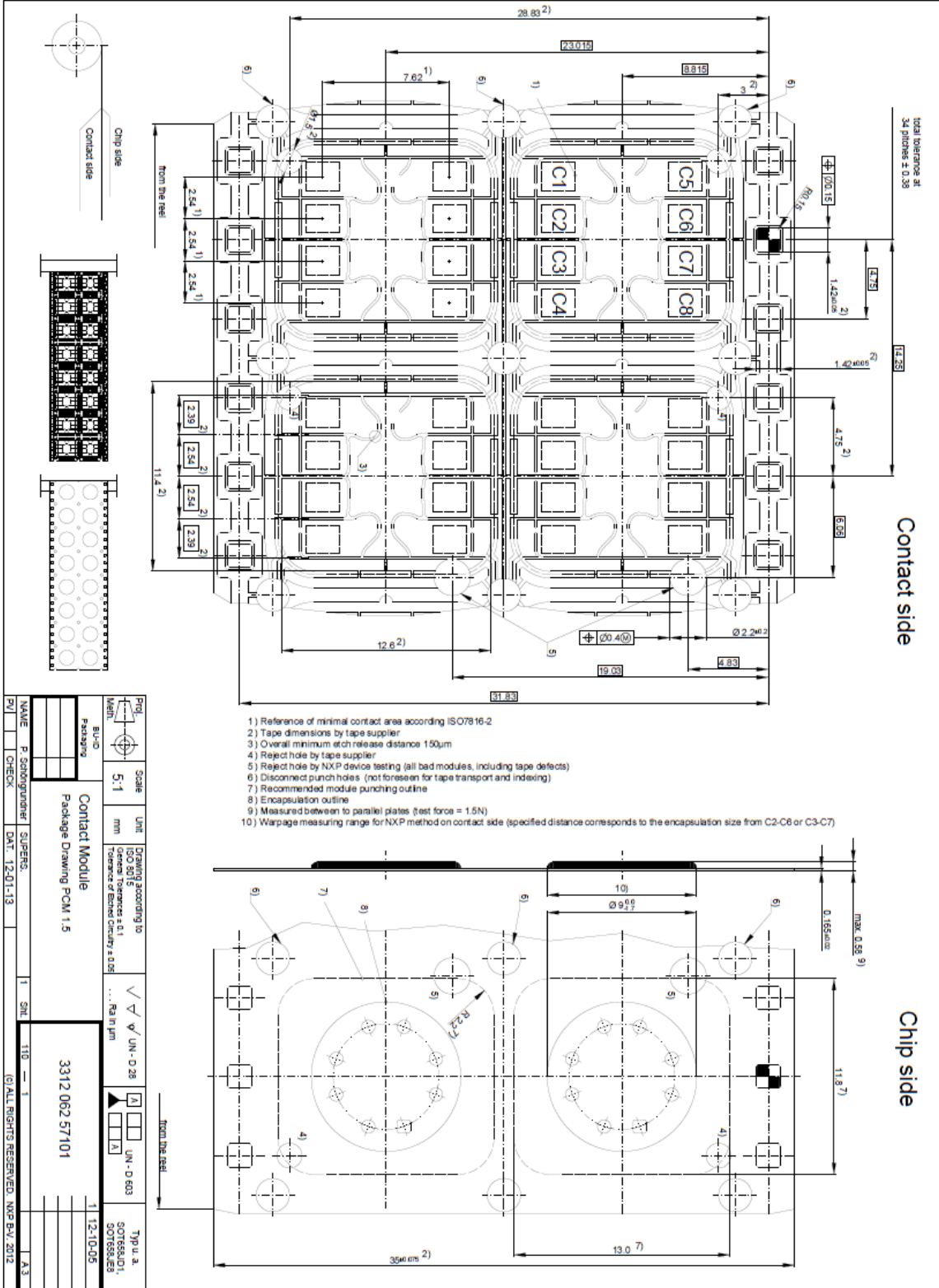


Figure 12. Package outline SOT658-1

11 Packing information

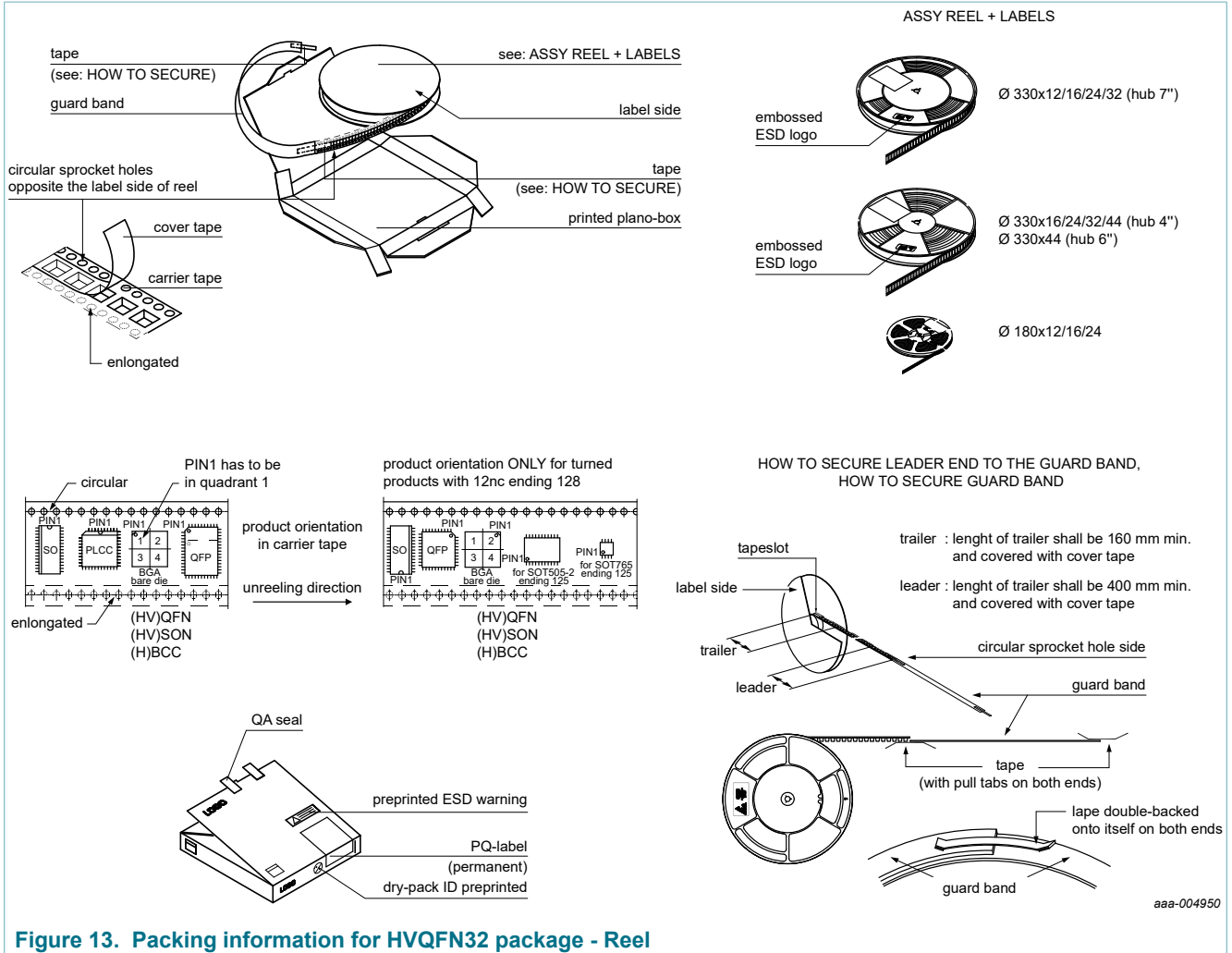


Figure 13. Packing information for HVQFN32 package - Reel



## 12 References

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- [1] Data sheet — MF4SAM3 MIFARE SAM AV3 secure access module product data sheet, Doc No. 3235\*\*<sup>3</sup>

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<sup>3</sup> \*\* denote the document version number

## 13 Revision history

Table 14. Revision history

| Document ID    | Release date               | Data sheet status  | Change notice | Supersedes |
|----------------|----------------------------|--------------------|---------------|------------|
| MF4SAM3_SDS    | 20190802                   | Product data sheet |               | --         |
| Modifications: | • Initial released version |                    |               |            |

## 14 Legal information

### 14.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**Tables**

|         |   |    |          |   |    |
|---------|---|----|----------|---|----|
| Tab. 1. | Ordering information .....  | 4  | Tab. 8.  | Electrical DC characteristics of TP1 and TP2 ...                    | 14 |
| Tab. 2. | Pin description PCM 1.5 MIFARE SAM AV3 .....                          | 6  | Tab. 9.  | Electrical characteristics of IC supply current ...                 | 16 |
| Tab. 3. | Pin description HVQFN32 MIFARE SAM AV3 .....                          | 7  | Tab. 10. | Electrical AC characteristics of IO1, IO2, IO3, CLK and RST_N ..... | 18 |
| Tab. 4. | Limiting values .....   | 8  | Tab. 11. | Electrical AC characteristics of TP1 and TP2 ...                    | 19 |
| Tab. 5. | Operating conditions .....  | 9  | Tab. 12. | Non-volatile memory characteristics .....                           | 20 |
| Tab. 6. | Electrical DC characteristics of Input/Output: IO1, IO2 and IO3 ..... | 10 | Tab. 13. | Non-volatile memory characteristics .....                           | 20 |
| Tab. 7. | Electrical DC characteristics of Inputs CLK and RST_N .....           | 12 | Tab. 14. | Revision history .....  | 26 |

**Figures**

|         |   |    |          |   |    |
|---------|---|----|----------|---|----|
| Fig. 1. | Block diagram .....   | 5  | Fig. 8.  | Input characteristic of CLK during IC reset .....   | 16 |
| Fig. 2. | Pin configuration PCM1.5 .....  | 6  | Fig. 9.  | External clock drive and AC test timing<br>reference points of CLK, RST_N, IO1, IO2<br>and IO3 (see and ) ..... | 19 |
| Fig. 3. | Pin configuration HVQFN32 .....   | 6  | Fig. 10. | Timing for I2C Slave bus .....  | 21 |
| Fig. 4. | Operating conditions over voltage range .....                                 | 9  | Fig. 11. | Package outline SOT617-3 .....  | 22 |
| Fig. 5. | Input characteristic of IO1, IO2, IO3 in<br>"quasi-bidirectional" mode .....  | 15 | Fig. 12. | Package outline SOT658-1 .....  | 23 |
| Fig. 6. | Input characteristic of IO1, IO2, IO3 in "weak<br>pull-up" input mode .....   | 15 | Fig. 13. | Packing information for HVQFN32 package<br>- Reel .....   | 24 |
| Fig. 7. | Input characteristic of CLK when the IC is not<br>in reset and of RST_N ..... | 16 |          |   |    |

**Contents**

**1 General description ..... 1**

**2 Features and benefits .....2**

2.1 Cryptography ..... 2

2.2 Communication ..... 2

2.3 Programmable logic (restricted feature) .....3

2.4 Security evaluation and certification ..... 3

2.5 New features ..... 3

**3 Ordering information ..... 4**

**4 Block diagram ..... 5**

**5 Pinning information ..... 6**

5.1 Pin description ..... 6

5.1.1 PCM1.5 pin configuration ..... 6

5.1.2 HVQFN32 pin configuration .....6

**6 Limiting values .....8**

**7 Recommended operating conditions .....9**

**8 Static characteristics ..... 10**

8.1 Measurement conventions ..... 10

8.2 Levels and currents ..... 10

8.3 General and ISO/IEC 7816 I/O interface at ISO/IEC 7816-3: A/5 V, class B/3 V or class C/1.8 V class operation ..... 16

**9 Dynamic characteristics ..... 18**

9.1 General, ISO/IEC 7816 I/O and ISO/IEC 14443 I/O interfaces ..... 18

9.2 Non-Volatile memory ..... 20

9.3 I2C Slave interface bus timing ..... 20

**10 Package outline .....22**

**11 Packing information .....24**

**12 References ..... 25**

**13 Revision history ..... 26**

**14 Legal information ..... 27**

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